WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device provided with a memory cell constructed of a floating-gate field-effect transistor, which has a control gate, a drain, a source and a floating gate and is able to electrically execute write and erase of information, and a read means, which has a first reference cell, the device comprising:

a second reference cell;

a threshold value comparing means for comparing a threshold value of the first reference cell with a threshold value of the second reference cell; and

a threshold value setting means for setting the threshold value of the first reference cell on the basis of a result of comparing the threshold value of the first reference cell with the threshold value of the second reference cell by the threshold value comparing means.

2. The nonvolatile semiconductor memory device as claimed in claim 1, wherein

the read means has the first reference cell and a first sense amplifier and reads the memory cell by using the first reference cell and the first sense amplifier, and

the threshold value comparing means has a second sense amplifier and compares the threshold value of the first reference cell with the threshold value of the second reference cell by means of the second sense amplifier.

3. The nonvolatile semiconductor memory device as claimed in claim 1, wherein

the read means has the first reference cell and a sense amplifier and reads the memory cell by using the first reference cell and the sense amplifier, and

the threshold value comparing means shares the sense amplifier owned by the read means as a sense amplifier for comparing the threshold value of the first reference cell with the threshold value of the second reference cell.

4. The nonvolatile semiconductor memory device as claimed in claim 1, comprising:

a plurality of second reference cells of different threshold values.

5. The nonvolatile semiconductor memory device as claimed in claim 1, wherein

if electrons are injected into the floating gate of the memory cell, a state in which the threshold value of the memory cell is raised is assumed to be a written state, and a state in which the threshold value of the memory cell is low is assumed to be an erased state,

then a target value of the threshold value of the first reference cell is intermediate between the threshold value in the written state and the threshold value in the erased state, and the threshold value of the second

reference cell is lower than the target value of the threshold value of the first reference cell.

6. The nonvolatile semiconductor memory device as claimed in claim 1, wherein

the threshold value of the second reference cell is lower than the target value of the threshold value of the first reference cell by a resolution of write of the threshold value setting means.

7. The nonvolatile semiconductor memory device as claimed in claim 1, wherein

the threshold value setting means is comprised of:

an internal control means for adjusting the threshold value of the first reference cell.